PROF. AKKARY DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING

AMERICAN UNIVERSITY OF BEIRUT

EECE 421 – COMPUTER Architecture

Quiz 1 – Fall 2012

NAME:

_____

ID: _____

INSTRUCTIONS:

- **THE DURATION OF THE EXAM IS TWO HOURS. NO TIME EXTENSION.**
- **THE EXAM IS CLOSED-BOOK/CLOSED-NOTES.**
- **USING CELL PHONES IS NOT ALLOWED IN THE EXAMINATION ROOM.**
- **WRITE YOUR NAME AND ID. NUMBER IN THE SPACE PROVIDED ABOVE.**
- **CIRCLE ONLY ONE ANSWER.**
- **READ THE QUESTIONS CAREFULLY BEFORE ANSWERING.**
- **IN SOME QUESTIONS, MORE THAN ONE CHOICE MAY BE A VALID ANSWER. CIRCLE THE BEST CHOICE YOU THINK IS THE MOST APPROPRIATE ANSWER TO THE QUESTION.**
- **ALL QUESTIONS ARE EQUALLY WEIGHTED.**
- **THERE IS NO PENALTY FOR WRONG ANSWERS.**
- **USE THE BACK PAGES FOR SCRATCH IF NEEDED**
- **CHECK THAT YOU HAVE A TOTAL OF 5 PAGES.**
- **NO QUESTIONS ARE ALLOWED.**
- **YOU CANNOT LEAVE THE EXAM ROOM FOR ANY REASON UNTIL YOU COMPLETE THE EXAM.**

1. Processor A has 50% more instructions IN A PROGRAM than processor B, but runs at 20% higher frequency and 20% lower CPI. Which processor is faster and by how much?

    a. A is 1.44 times faster than B.
    b. B is 1.44 times faster than A.
    c. A and B have about the same speed.
    d. B is 1.1 times faster than A.
    e. A is 1.1 times faster than B.

2. Processor A is 20% faster on 3 benchmarks, 10% slower on 2 benchmarks and 40% slower on 1 other benchmark. Using Arithmetic mean, processor A is faster than processor B.

    a. True
    b. False

3. Spec 2006 benchmarks are used to measure performance of server computers.

    a. True
    b. False

4. Which of the following statements about pipelines is False?

    a. In-order issue pipelines may encounter R after W hazards but not W after W hazards.
    b. In-order issue pipelines do not encounter W after R hazards.
    c. In-order issue, out-of-order completion pipelines may encounter R after W hazards and W after W hazards.
    d. Out-of-order issue pipelines may encounter R after W, W after W and W after R hazards.
    e. Register renaming eliminates W after W hazards, W after R hazards but not R after W hazards.

5. The only way to deal with W after W and W after R hazards is to do register renaming.

    a. True.
    b. False.

6. Multi-cycle execution units cause R after W hazards.

    a. True.
    b. False.

7. Multi-cycle execution units cause W after W hazards.

    a. True.
    b. False.

8. Multi-cycle execution units cause W after R hazards.

    a. True.
    b. False.

9. If 12% of total processer power is static power. How much percent reduction in total power results from reducing the voltage from 1.2 volt to 1 volt, assuming that the frequency is kept the same?

    a. 10%
    b. 21%
    c. 29%
    d. 45%
    e. None of the above

10. A design team decides to improve a processor that emulates floating point computations in software by implementing floating point hardware functional units. If the floating point hardware is 10 times faster than software emulation, and the floating point hardware is used 30% of the time during a program execution. How much overall speedup is achieved due to the hardware improvement?

    a. 1.1
    b. 1.4
    c. 3.7
    d. 4.1
    e. None of the above

11. A RISC ISA processor is always slower than a register-memory ISA processor because it requires a larger number of instructions.

    a. True
    b. False

12. A small number of instructions are used most of the time during the execution of a typical RISC program.

    a. True
    b. False

13. A small number of instructions are used most of the time during the execution of a typical CISC program.

    a. True
    b. False

14. Because RISC instructions are simple and require less hardware to implement, RISC ISAs usually have a larger variety of instructions than CISC ISAs.

    a. True
    b. False

15. If the address of an integer variable in a 32-bit RISC processor is 240, the integer is aligned in memory.

    a. True
    b. False

16. Which of the following statements is False?

    a. Tomasulo's algorithm handles W after W hazards by delaying the second write in the reservation station until the first write instruction completes execution.
    b. Tomasulo's algorithm handles Read after write hazards by delaying the read instruction in the reservation station until the write instruction completes execution.
    c. Tomasulo's algorithm handles execution units resource hazard between two instructions by delaying one instruction in the reservation station until the other completes execution.
    d. Tomasulo's algorithm handles reservation stations resource hazards by delaying instructions at the deocde stage.
    e. The common data bus in Tomasulo's algorithm is connected to all reservation stations.

17. Which of the following statements is True?

    a. Tomasulo's algorithm avoids W after R hazards by writing results into the register file in-order.
    b. Tomasulo's algorithm avoids W after R hazards by stalling at the decode stage.
    c. Tomasulo's algorithm avoids W after R hazards using tag comparators in the register file.
    d. Tomasulo's algorithm avoids W after R hazards by broadcasting the result tag frm the execution unit to all reservation stations.
    e. None of the above is True.

18. Which of the following statements is True?

    a. Register windows are used to handle register renaming.
    b. Register windows are used to handle loops execution.
    c. Register windows are used to handle procedures execution.
    d. Register windows are used to handle delayed branches.
    e. None of the above is True.

19. Which of the following statements is True?

    a. A delayed branch is a branch that is delayed due to R after W hazards.
    b. A delayed branch sometimes increases the number of instructions in a program.
    c. A delayed branch sometimes decreases the number of instructions executed in a program.
    d. A delayed branch always executes after the next instruction in program memory executes.
    e. None of the above is True.

20. Select the True statement:

```
Mul     R1, R2, R3
Add     R5, R1, R4
Ld      R2, 0(R4)
Sub     R5, R1, R5
St      R1, 0(R1)
```

In this code there exists:

a. 4 RAW, 1 WAW and 1 WAR dependences
b. 3 RAW, 2 WAW and 3 WAR dependences
c. 3 RAW, 1 WAW and 1 WAR dependences
d. 4 RAW, 2 WAW and 2 WAR dependences
e. None of the above

21. If the address of a long integer in a 32-bit RISC processor is 548, the integer is aligned in memory.

a. True
b. False